IN THE CLAIMS

1. A method for estimating reference frequency drift in a navigation receiver, the method comprising the steps of:

5   associating a PDC handset subject to standby mode with a navigation receiver;

sampling a VCO burst information that is received by said PDC handset;

running a numeric controlled oscillator (NCO) at a

10   nominal frequency;

periodically adjusting said NCO with samples obtained in the step of sampling;

correlating both in-phase and quadrature-phase outputs of said NCO; and

15   computing a navigation receiver reference frequency drift estimate from information derived in the step of correlating.

2. The method of claim 1, further comprising the step of:

20   building a reference sinewave from data output by said NCO and passing such as updates to the step of correlating.

3. A circuit for estimating reference frequency drift in

25   a navigation receiver, comprising:

a numeric controlled oscillator (NCO) for periodically receiving an NCO_value on which an NCO output frequency depends;

a first lookup table for approximating a sinewave

30   from an inphase version of said NCO output frequency;

a first mixer connected to an output of the first lookup table and for combining it with a gated master clock

(MCLK) signal, and providing further for an I-mix signal output;

an I-correlator for correlating said I-mix signal output and having an I-correlation output;

5   a second lookup table for approximating a cosine wave from a quadrature phase version of said NCO output frequency;

a second mixer connected to an output of the second lookup table and for combining it with said gated master clock 10   (MCLK) signal, and providing further for a Q-mix signal output;

a Q-correlator for correlating said Q-mix signal output and having an Q-correlation output; and

a drift estimate output comprising said I-15   correlation and Q-correlation outputs.

4. The circuit of claim 3, further comprising:

an NCO value holding latch for receiving a data write from a firmware control program, and connected to gate 20   an MCLK signal to the first and second mixers.

5. The circuit of claim 3, further comprising:

an I-latch and a Q-latch providing for a register of said I-correlation and Q-correlation outputs to a data read 25   from a firmware control program.